

Application No.: 10/065,212
Amendment dated February 08, 2007
Amendment made in response to Office Action dated November 08, 2006

REMARKS AND ARGUMENTS

Allowed claims

The Examiner has allowed claims 2-10, 13-20 and 22-25. These claims are patentable over the cited art of record.

Rejection under 35 USC §102

Claims 1 and 11-12 are rejected under 35 USC § 102(e) as being anticipated by US Patent 2002/0065997 A1 (Hsu et al.). With respect to claim 1, the Examiner states that Hsu et al. teaches a cache memory as recited by claim 1. The Examiner directed the Applicant to paragraph [0052] of Hsu et al. Applicant respectfully disagrees.

Claim 1 as presented recites "a cache memory coupled to said first and second access ports, wherein during a read operation to the memory cell array to obtain read data through one of said first and second access ports, the cache memory provides the read data if the read data is contained therein or the memory cell array provides the read data if the read data is not contained in the cache memory..." As such, claim 1 requires that during a read operation to the memory cell array, the cache is first checked to determine if it contains the read data. In the case where the cache contains the read data, the read data is provided to the processor. If not, the processor retrieves the read data from the memory cells.

It is well established that all limitations in a claim must be afforded patentable weight for determining anticipation. *See, e.g., In re Ludtke*, 441 F.2d 660, 169 USPQ 563, 566 (C.C.P.A. 1971); and *In re Atwood*, 354 F.2d 365, 148 USPQ 203, 210 (C.C.P.A. 1966). Paragraph [0052] of Hsu et al. to which the Examiner directed the Applicant, only discusses that memory array having multiple ports are useful for applications which require massive (e.g., block) data transfers between processors or between the core and cache memories. *See* Hsu et al., paragraph [0052]. This is the only portion of Hsu et al. which refers to a cache memory. Hsu et al. nowhere teaches or suggests that read data is provided by the cache memory during a read operation to the memory array if the cache contains the

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read data or that the read data is provided by the memory array if the read data is not contained in the cache memory. It only describes block data transfers between the core memory and cache memory.

Furthermore, inherency may not be established by probabilities or possibilities. The missing limitations or functions must necessarily result from the prior art reference. The mere fact that a certain thing may result is not sufficient. *See, e.g., In re Olerich*, 666 F.2d 578, 212 USPQ 323 (C.C.P.A. 1981); and *In re King*, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986). Applicant submits that Hsu et al. nowhere teaches or suggests how the cache functions during a read operation to the memory. The mere fact that Hsu et al. mentions that block data transfers between the core and cache memory does not teach, suggest or necessarily result in checking the cache memory during a read operation to the memory to see if the read data is contained therein. Applicant therefore submits that claim 1 is patentable over Hsu et al. Since claims 11 and 12 are dependent directly or indirectly on claim 1, these claims are also patentable. As such, Applicant respectfully requests withdrawal of the rejection based on 35 USC § 102(e)

Newly added claim 26 recites an IC comprising a memory cell array having a plurality of memory cells, wherein each memory cell includes at least a first port and at least a second port, the first and second ports of the memory cells forming at least first and second access ports of the memory cell array for accessing the memory cells. The IC further comprises a cache memory coupled to said first and second access ports and a refresh control circuit for performing refresh operations for said memory cells, wherein during a conflict between a read operation to the memory cell array and a refresh operation, the cache memory provides read data if the read data is contained therein or the read operation is stalled until the conflict is over if the read data is not contained in the cache memory.

Applicant submits that Hsu et al. nowhere teaches or suggests that during a conflict between a read operation to the memory cell array and a refresh operation, the cache memory provides read data if the read data is contained therein or the read operation is stalled until the conflict is over if the read data is not contained in the cache memory. Therefore, Applicant submits that claim 26 is also patentable over Hsu et al. or the cited art of record, alone or in combination.

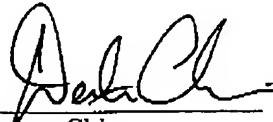
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Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance and the issuance of a formal Notice of Allowance at an early date is respectfully requested. Should the Examiner believe that a telephone conference would expedite prosecution of this application, please telephone the undersigned attorney at his number set out below.

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Respectfully submitted,



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